IN THE SPECIFICATION:

Please replace paragraphs [0008], [0018], [0038], [0039], [0040], [0041], [0042], [0048], [0054], [0062], [0078] and the Abstract of the Specification with the following paragraphs (a marked-up version of the specification changes is included at the end of this Amendment):

[0008] After the instructions have been fetched by a fetch unit, passed through a decode and branch prediction unit, stored in the instruction queue and have been renamed in a renaming unit they are stored in a part of the IWB called reservation station. From the reservation station the instructions may be issued out to a plurality of instruction execution units abbreviated herein as IEU, and the speculative results are stored in a temporary register buffer, called reorder buffer, abbreviated herein as ROB. These speculative results are committed (or retired) in the actual program order thereby transforming the speculative result into the architectural state within a register file, a so-called Architected Register Array, further abbreviated herein as ARA. In this way it is assured that the out-of-order processor (also referred to herein as an outprocessor) with respect to its architectural state behaves like an in-order processor.

[0018] It is thus an objective of the present invention to reduce the pipeline length in performance-critical cases.

[0038] It is contemplated that operations described herein can be implemented in either hardware or software. In this basic approach at least the instructions with all source data in an architected state (data resides in the register file) are covered by the dependency check.

[0039] Further, when the step of generating a "no dependency" signal comprises the step of comparing a plurality of logic target register addresses and the logic source register address of the current instruction, in case of a match, and the step of generating a dependency for the respective source register (and thereby the instruction becomes dependent on another older instruction), the simplest way to determine "no dependency" is disclosed because this corresponds straight-forward to the definition of dependency.

[0040] Further, when "valid"-bits of non-target registers stored in a storage as e.g., the reorder buffer, which is associated with speculatively calculated instruction result data are involved into the no generation, then the advantage is that additional information is made available saying if a respective target register data stored in the reorder buffer is valid or not. Thus, the no-dependency signal generation covers more cases, i.e., the speculatively calculated cases too, i.e., the method is more effective.

[0041] Further, the concepts of the present invention can be applied as well in a mapping-renaming scheme. Then a mapping table entry is addressed with a logical source register address of the current instruction, whereby the mapped physical target register address is determined, then, a committed-status-flag in said entry is read, and thus, it is known where the data resides, in the ROB (non-committed), or already in the ARA (committed), then, the logic target register address and the logic source register address of the current instruction are compared, and in case of a match, a dependency-signal is generated for the respective source register.

[0042] In case of a content-addressable memory (CAM) renaming scheme, according to a preferred embodiment, the means for determining the dependency of a current instruction comprises a compare logic in which all instructions to be checked for dependency are involved, and a post-connected OR gate.

[0048] The fetch unit dispatches up to 4 instructions each cycle to the IWB in program order. The IWB pipeline starts with renaming--510--the up to 4 dispatched instructions. The renaming process, compares the source registers with the target registers of previous instruction and in case of a match, i.e., a dependency is found, then, the ROB entry of the target is assigned to the source register. Furthermore, new ROB entries are allocated for the target register of the instruction. In this ROB entry the speculative results will be stored after execution.

[0054] For the case that there is no dependency (RSEL (0 . . . 63)="00 . . . 00") the "read_ARA" is switched ON by the ROB causing the operand data to be read from the ARA (addressed by the logical address). This ends the "read ROB" cycle.

[0062] As may be apparent from the above illustration and description the present invention discloses the introduction of a "no_dependency" signal that directly tells the select logic 418 that the renamed logic will have all its source data available. In this way, the rename/issue part of the pipeline is reduced to three stages as shown in FIG. 6 where the same reference signs apply.

[0078] Further variations are possible such as for example the used of a mapping table based renaming scheme as discussed in the previous section, and a single register file in which an instruction is committed by setting a commit bit for the register file entry (rather then copying the data from the ROB to the ARA data file). This however does not modify the objective of the invention by reducing the pipeline length by the generation of a "no_dependency" signal for the cases were the source data is directly available for the instruction. In this latter case, the validity of the data can be derived from including the valid bit into the "no_dependency" generation.

[ABST] A method and system for operating a high frequency out-of-order processor with increased pipeline length. A new scheme is disclosed to reduce the pipeline by the detection and exploitation of so called "no dependency" for an instruction. A "no dependency" signal tells that all required source data is available for the instruction at least one cycle before the source data valid bit(s) are inserted into the issue queue. Therefore, one or more stages of the pipeline are bypassed.